

**PATENT APPLICATION**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Attn: OIPE

Nabuo KARAKI

Application No.: 10/820,841

Docket No.: 119408

Filed: April 9, 2004

For: SEMICONDUCTOR INTEGRATED CIRCUIT, ELECTRONIC EQUIPMENT, AND  
TRANSISTOR BACK-GATE VOLTAGE CONTROL METHOD

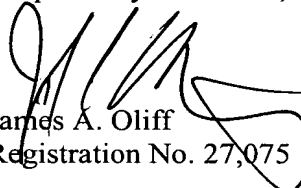
**REQUEST FOR CORRECTION OF PALM RECORDS**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Attached is a photocopy of the original filing receipt on which errors have been corrected in red. These errors are being brought to the attention of the Patent and Trademark Office so that it may correct its records. A Supplemental Application Data Sheet is attached.

Respectfully submitted,

  
James A. Oliff  
Registration No. 27,075

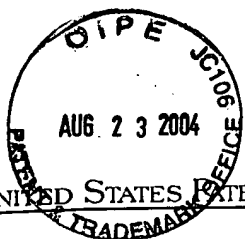
Joel S. Armstrong  
Registration No. 36,430

JAO:JSA/nxy

Date: August 23, 2004

**OLIFF & BERRIDGE, PLC**  
**P.O. Box 19928**  
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<p><b>DEPOSIT ACCOUNT USE AUTHORIZATION</b> Please grant any extension necessary for entry; Charge any fee due to our Deposit Account No. 15-0461</p>
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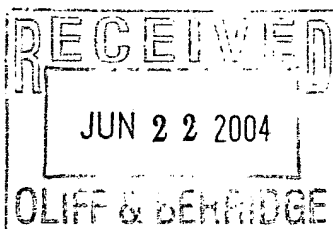


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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/820,841	04/09/2004	2811	856	119408	8 ✓	19 ✓	4 ✓

25944  
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CONFIRMATION NO. 8476

FILING RECEIPT



\*OC000000013002609\*

Date Mailed: 06/21/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Nobuo Karaki, ~~Suwa-shi~~, JAPAN; **Matsumoto-shi**

Assignment For Published Patent Application

Seiko Epson Corporation, Tokyo, JAPAN;

Domestic Priority data as claimed by applicant

Foreign Applications

JAPAN 2003-112088 04/16/2003

JAPAN 2004-044584 02/20/2004

If Required, Foreign Filing License Granted: 06/19/2004

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

Semiconductor integrated circuit, electronic equipment, and transistor back-gate voltage control method

**Preliminary Class**

257

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Title 37, Code of Federal Regulations, 5.11 & 5.15**

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